High-Accuracy Digital 5-Bit 0.8-2 GHz MMIC RF Attenuator for Cellular Phones

Noyan Kinayman*, Marco Bonilla**, Mark F. Kelcourse**, Jack Redus**, Kevin Anderson**

*M/A-COM, Corporate Research and Development, 1011 Pawtucket Blvd., Lowell, MA 01854, USA

**M/A-COM, ISBU, 100 Chelmsford Street, Lowell, MA 01853, USA

Abstract — **High-accuracy digital MMIC RF attenuator for cellular phones is presented. Designing high accuracy digital MMIC RF attenuators is challenging due to non-ideal characteristics of the transistor switches used in the attenuator and other parasitic effects. This problem can be circumvented by simultaneous optimization of the attenuator circuit at every possible input bit configuration. Without this optimization scheme, it would be extremely difficult to compensate the non-ideal transistor switch characteristics to achieve high accuracy. A design methodology will be presented.**

I. INTRODUCTION

Digital MMIC RF attenuators are widely used in modern communication devices and systems, especially in cellular-phones. Cellular-phone manufacturers sometimes require very high accuracy digital attenuators, which deserve significant design effort. In the literature, there are examples of digital RF attenuators explaining the design procedure in various aspects [1-3]. However, the accuracies of digital RF attenuators in attenuation linearity and bit-to-bit variations have not been addressed satisfactorily before. In this paper, we are going to address this issue and present a high-accuracy 0.8-2 GHz RF digital attenuator for cellular phones. Measurement results of the manufactured attenuators will be also presented.

There are mainly two important accuracy characteristics of a digital attenuator that can be given as follows: *i.)* deviation from the ideal attenuation response (attenuation linearity), and *ii.)* difference between the consecutive attenuation values (bit-to-bit variation). Figure 1 shows the graphical explanation of these accuracy characteristics. The deviation from the ideal response specifies how closely the attenuator should follow the desired attenuation curve. Normally, the attenuation curve is a straight line with a reference insertion loss. Therefore this specification should ideally be zero. The second specification is the difference between the consecutive attenuation values. This specification should ideally be constant. The total number of bits used to control the attenuator determines this value. For instance, for a digital attenuator in the range of 0-15.5 dB, which has a 5 input control bits, has a 0.5 dB attenuation steps. Therefore, there should be 0.5 dB between any two consecutive attenuation values. Any deviation from this value is an error. Note that the first and second specifications are independent each other by definition and should be satisfied simultaneously in a high-accuracy digital RF attenuator.

In the next section, we will present the high-accuracy digital RF attenuator providing the simulation and measurement results. Finally, conclusions are given.

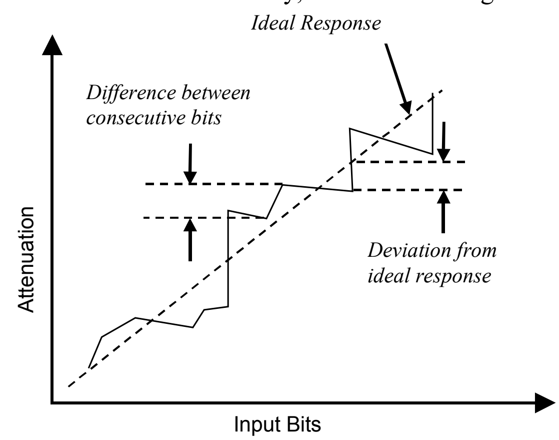

Figure 1: Graphical explanation of the two important accuracy characteristics of digital RF attenuators.

II. DESIGN OF THE ATTENUATOR

Digital MMIC RF attenuators are designed by using resistive attenuator pads (Pi- or T-type) and transistor switches to insert the pads into RF path depending on the input bits. Although the fundamental design procedure is relatively straightforward, what makes the design of high accuracy MMIC RF attenuator challenging is the non-ideal characteristics of the transistor switches employed, parasitic effects, and the process variations from wafer to wafer.

Under ideal conditions of the transistor switches (i.e., zero turn-on resistance and infinite turn-off resistance), it is relatively easy to design a digital RF attenuator with high accuracy. However, non-zero turn-on and finite turn-off resistance values of the transistor switches and other parasitic effects (such as package lead inductances, FET capacitances, etc.) make the design process difficult if one wants achieve very high accuracy at every input bit configuration. This is due to fact that the loads seen by the each attenuator pad changes each time as the input bit changes because of the non-ideal characteristics of the switches. Therefore, the assumption of constant load and source impedance while determining the impedance values of the resistors in the attenuator pads is violated as the input bits of the attenuator are changed. Besides, due to limitations on the number of control bits and chip real estate, sometimes it is necessary to use single resistors instead of balanced T- or Pi-pads in the lower order attenuation bits. This makes the design process further difficult to achieve high accuracy. The solution of this problem is to simultaneously optimize the attenuator circuit with the inclusion of non-ideal switch characteristics at every possible input bit configuration. Note that simultaneous optimization is the key point to achieve high accuracy. However, this cannot be done by brute force due to high number of possible combinations. For instance, for a 5-bit attenuator, there are 32 different possible input combinations. It is clearly unfeasible to duplicate the circuit 32 times in the circuit simulator with different settings and try to optimize 32 different circuits at the same time.

The design steps for the high accuracy attenuator is as follow: First, the initial values of the resistors for each pad are found from the standard attenuator formulas for constant 50-Ohm input and output impedance. Second, the whole circuit is optimized using a suitable circuit simulator at every possible bit combination to achieve very high attenuation accuracy and good bit-to-bit variations. The circuit simulator used here is the ADS™ v1.3 by Agilent. ADS™ has the capability of optimizing the circuit while sweeping independent variables. This is a very powerful and useful feature in designing of RF attenuator circuits. In our case, this feature is used to optimize the attenuator while sweeping the input bits. By this way, the whole circuit is optimized simultaneously for every possible input bit configuration in an automatic manner. The optimization parameters can be selected as the reflection loss, accuracy in the attenuation and accuracy in the bit-to-bit variation.

In this work, we have employed a series topology for the attenuator where all the attenuator pads are connected in series as shown in Figure 2 (M/A-COM part number: AT280). The transistor switches are MESFET switches with the following process parameters: C_{sheet}=120 pF/mm, $V_{pinch\ off}$=-2.5 to -1.7 V, I_{dss}=175 to 350 mA/mm, R_{on}=2.0 to 3.7 Ohm/mm, R_{sheet}=160 to 190 Ohms/square, and $R_{contact}$=0.085 Ohms. Selection of the transistor type is not critical since their effect on the performance will be taken into account by the optimization algorithm. Therefore, any switch (electronic, electromechanical, or MEMS) can be used in this design scheme as long as good circuit models for the switches are available. We have used single resistors for 0.5 and 1 dB attenuator pads and suitable T- and Pi-pads for 2-, 4-, and 8-dB attenuator pads.

In order to give an idea about the resistor values of the pads, Table 1 is provided here. The table shows the initial resistor values and optimum resistor values for the attenuator pads. Note that ideally the attenuator pads would be symmetric if the input and output load impedances were the same. However, as explained above, the non-ideal switch characteristics change the loading of the pads as a function of input bits. Therefore, one might expect that the optimum values of the resistors are not symmetric. In fact, after the optimization process, it was seen that this is the case as shown in Table 1.

Simulation results of the designed attenuator in the frequency range 0.8-2 GHz are given in Figure 3 through Figure 6. In the figures, the input bits are shown in the horizontal axis (attenuator setting). The RF attenuator was optimized at 1.4 GHz yielding very-high accuracy at this frequency as shown in Figure 5 and Figure 6. For instance, the bit-to-bit variation (delta) at 1.4 GHz is better than +/- 0.03 dB for every possible bit combination. Attenuation accuracy and VSWR are better than +/- 0.03 dB and 1.3, respectively, for every possible bit combination at the same frequency.

Figure 7 through Figure 10 shows measurement results of the manufactured attenuators for three different samples at two test frequencies. The bit-to-bit variation (delta) and the attenuation accuracy are better than +0.15/-0.1 dB and +0.1/-0.2 dB, respectively, for every possible bit combination. The VSWR of the attenuators are better than 1.5. It is interesting to note that most of error in the bit-to-bit variation occurs when the 8-dB pad is turned on. However, the same pad also helps keep tracking the ideal attenuation curve. The difference between the measured and the simulated results is most probably due to the inaccuracies in the FET switch models.

III. CONCLUSION

In this paper, a high-accuracy 5-bits 0.8-2 GHz RF digital attenuator for cellular phones is presented. The bit-to-bit variation (delta) and the attenuation accuracy are better than +0.15/-0.1 dB and +0.1/-0.2 dB, respectively.

The design is based on the simultaneous optimization of the attenuator pads at every possible input bit combination. In order to achieve this, one must use a circuit simulator, which has the capability of making optimization while sweeping one or more independent variables. The technique is generic and not limited to a specific topology, switch type, or MMIC process.

ACKNOWLEDGEMENT

The authors acknowledge the assistance and help of Timothy Fox, Ed Woytaszek, Ralph Howard, Don Carter, and John Dames.

REFERENCES

[1] D. Krafcsik, F. Ali and S. Bishop, "Broadband, Low-Loss 5- and 6-Bit Digital Attenuators," *IEEE MTT-S Int. Microwave Symp. Digest,* vol. 3, pp. 1627-1630, 1995.

[2] J. Bayruns, P. Wallace and Scheinberg. "A Monolithic DC-1.6GHz Digital Attenuator," *IEEE MTT-S Int. Microwave Symp. Digest,* vol. 3, pp. 1295-1298, 1989.

[3] C. Sarkissian, M. Delmond, E. Loporte, E. Rogeaux, and M. Soulard, "Ku-Band 6-Bit Digital Attenuator with Integrated Serial to Parallel Converter," *IEEE MTT-S Int. Microwave Symp.,* pp. 1915-1918, 1999.

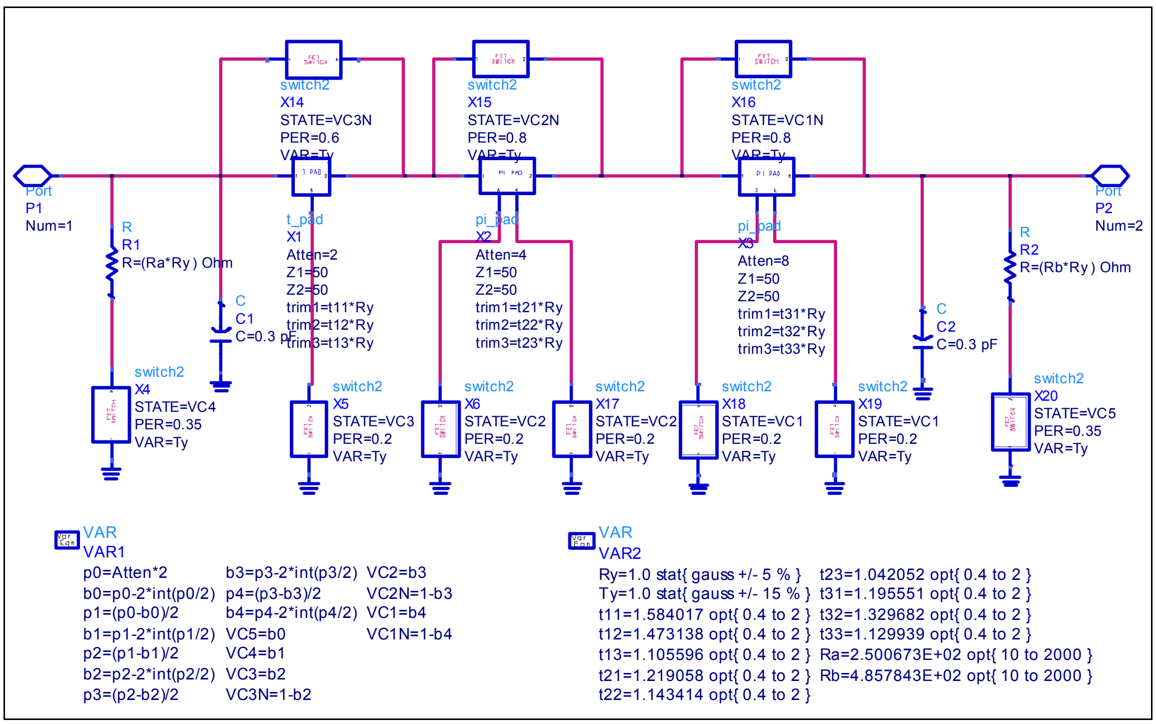

Figure 2: Simplified topology of the digital RF attenuator (M/A-COM part number: AT280). The attenuation values for the pads starting from left are as follows: 0.5 dB, 2 dB, 4 dB, 8 dB and 1 dB. Note that to save from the control inputs, single resistors are used for the 0.5 and 1 dB pads. The variable blocks on the bottom are used to control the transistor switches according to input (sweep parameter) value.

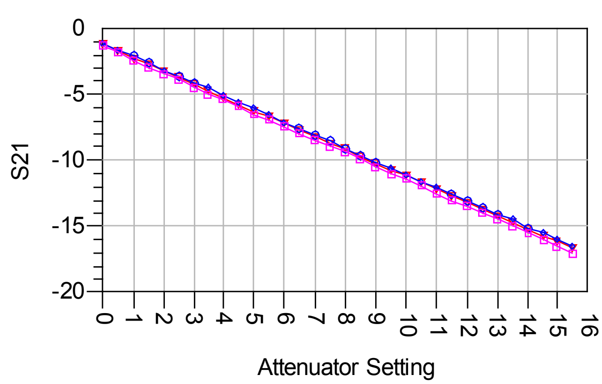

Figure 3: Simulated insertion loss of the attenuator (*circle*: 0.8 GHz, *triangle*: 1.4 GHz, *square*: 2.0 GHz).

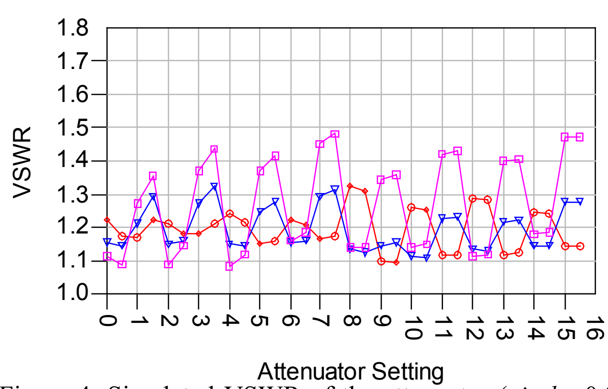

Figure 4: Simulated VSWR of the attenuator (*circle*: 0.8 GHz, *triangle*: 1.4 GHz, *square*: 2.0 GHz).

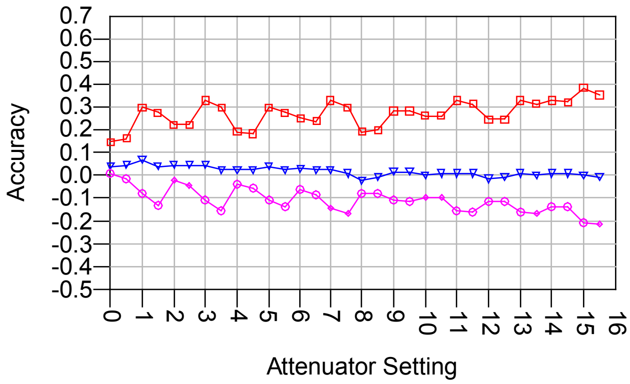

Figure 5: Simulated accuracy of the attenuator (*circle*: 0.8 GHz, *triangle*: 1.4 GHz, *square*: 2.0 GHz).

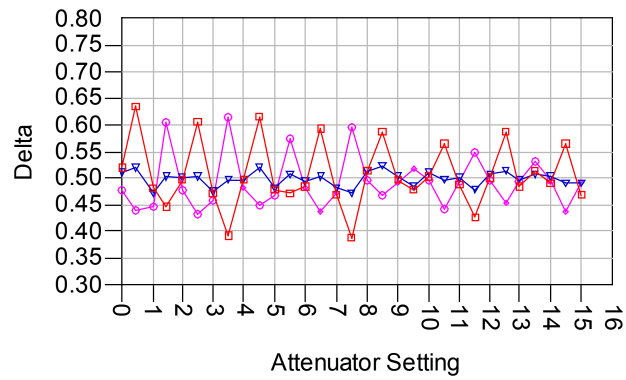

Figure 6: Simulated bit-to-bit variation (delta) of the attenuator (*circle*: 0.8 GHz, *triangle*: 1.4 GHz, *square*: 2.0 GHz).

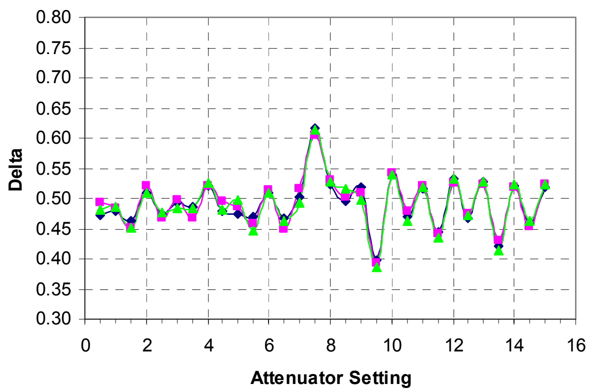

Figure 7: Measured bit-to-bit variation (delta) of three different samples at 1.0 GHz.

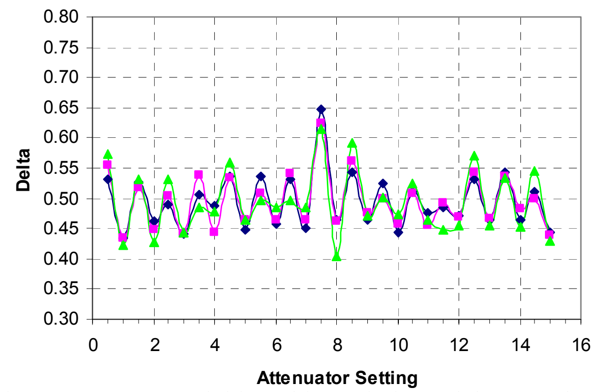

Figure 8: Measured bit-to-bit variation (delta) of three different samples at 2.0 GHz.

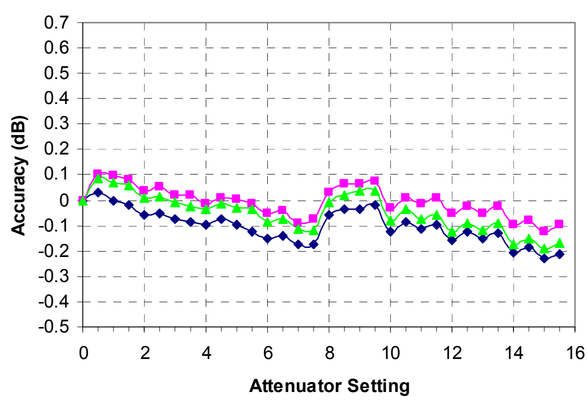

Figure 9: Measured attenuation accuracy of three different samples at 1.0 GHz. The insertion loss is normalized for each attenuator.

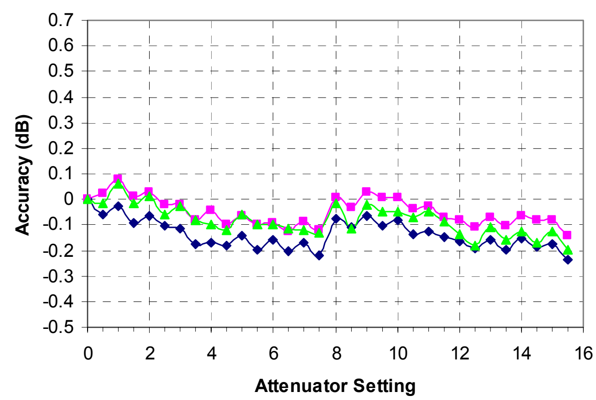

Figure 10: Measured attenuation accuracy of three different samples at 2.0 GHz. The insertion loss is normalized for each attenuator.

Table 1: Nominal and Modified Resistor Values (Ohm) for the Attenuator Pads. Trimming Coefficients Are Determined by the Optimization Algorithm and Nominal Resistor Values Are Multiplied With These Values to Determine the Modified Resistor Values. Note That After Optimization, the Modified Resistor Values Are Not Symmetric.

Attenuation		Pad	Nominal Resistor Values			Trimming Coefficients			Modified Resistor Values		
2dB	1.58	T	5.73	215.24	5.73	1.58	1.11	1.47	9.1	238.1	8.4
4dB	2.51	Pi	220.97	23.85	220.97	1.22	1.04	1.14	269.4	24.9	252.6
8dB	6.31	Pi	116.14	52.84	116.14	1.20	1.13	1.33	138.9	59.7	154.5